

Description

NPN DARLINGTON ESD PROTECTION CIRCUIT

BACKGROUND OF INVENTION

[0001] 1.Field of the Invention

[0002] The present invention relates to an electrostatic discharge protection circuit, and more particularly, to an NPN Darlington ESD protection circuit.

[0003] 2.Description of the Prior Art

[0004] Static electricity is everywhere, because it is very possible to form static electricity by rubbing together any two bodies of different materials. When a body having static electricity touches metal pins of an IC, it will discharge high voltage to damage the internal circuit through the metal pins of the IC. Electrostatic discharge (ESD) will cause the electrical system to lose efficacy. When electrostatic discharge occurs, an electrostatic discharge protection circuit can act before a pulse of electrostatic discharge arrives at

the internal circuit to eliminate the high voltage immediately and decrease the damage by the electrostatic discharge. Simultaneously, the protection circuit also has to sustain the energy of the electrostatic discharge and not damage itself. Additionally, the protection circuit acts only when electrostatic discharge occurs to prevent electrostatic discharge from influencing normal operations.

[0005] Please refer to Fig.1. Fig.1 is a schematic view of a BJT ESD protection circuit according to the prior art. As shown in Fig.1, in a BiCMOS application, an NPN BJT is used as an ESD protection circuit. A base of the NPN BJT is floating, an emitter is grounded, and a collector is connected to an input pad or a VDD pad of an internal circuit. When the input pad or the VDD pad of the internal circuit is influenced by an electrostatic discharge, the NPN BJT operates in breakdown to ground current of the electrostatic discharge. The advantage of using the open-base NPN BJT as an ESD protection circuit is the small input capacitance of the NPN BJT. However, the NPN BJT has a current limitation such that the protection effect is poor, this being the shortcoming of using the open-base NPN BJT as the protection circuit.

[0006] Please refer to Fig.2. Fig.2 is a schematic view of a MOS

ESD protection circuit according to the prior art. As shown in Fig.2, a MOS is used as an ESD protection circuit. A gate of the MOS is connected to a source, the source is grounded, and a drain is connected to an input pad or a source pad of an internal circuit. When the input pad or the source pad of the internal circuit is influenced by an electrostatic discharge, the MOS turns on to ground current of the electrostatic discharge. The advantage of using a gate-grounded MOS as an ESD protection circuit is better ESD protection because the MOS is capable of handling a large current. However, the shortcoming of using gate-grounded MOS as an ESD protection circuit is that the MOS has a larger input capacitance, so the operation speed of the MOS is too slow in providing complete protection to the internal circuit.

[0007] According to the above-mentioned ESD protection circuits, using an open-base NPN BJT as an ESD protection circuit has a fast operation speed but a poor ESD protection effect, and using gate-grounded MOS as an ESD protection circuit has a better ESD protection effect but an operation speed that is limited because of the larger input capacitance.

[0008] For other related techniques please refer to U.S. Patent

Numbers 5,530,612, 5,986,863, 6,028,758, 6,320,735, and 6,400,540, U.S. filing Patent Number 20020027755A1, and European Patent Numbers 651,490 and 477,429.

SUMMARY OF INVENTION

- [0009] It is therefore a primary objective of the claimed invention to provide a NPN Darlington ESD protection circuit to solve the above-mentioned problems.
- [0010] According to claimed invention, an electrostatic discharge protection (ESD) circuit includes an NPN Darlington circuit and an n-type metal oxide semiconductor (NMOS) transistor. A drain of the NMOS transistor is connected to an input end of the NPN Darlington circuit. A source of the NMOS transistor is connected to a control end of the NPN Darlington circuit. A gate of NMOS transistor is connected to an output end of the NPN Darlington circuit.
- [0011] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

- [0012] Fig.1 is a schematic view of a BJT ESD protection circuit according to the prior art.
- [0013] Fig.2 is a schematic view of a MOS ESD protection circuit according to the prior art.
- [0014] Fig.3 is a schematic view of an ESD protection circuit according to the present invention.
- [0015] Fig.4A and Fig.4B are cross-sectional views of a BiCMOS structure of an ESD protection circuit according to the present invention.
- [0016] Fig.5A and Fig.5B are cross-sectional views of a CMOS structure of an ESD protection circuit according to the present invention.
- [0017] Fig.6 is a schematic view of an ESD protection circuit connected a source pad according to the present invention.
- [0018] Fig.7 is a schematic view of a complementary ESD protection circuit according to the present invention.

DETAILED DESCRIPTION

- [0019] Please refer to Fig.3. Fig.3 is a schematic view of an ESD protection circuit according to the present invention. The present invention ESD protection circuit 10 comprises an NMOS transistor 12, a first NPN BJT 14, a second NPN BJT 16, a first resistor 18 and a second resistor 20. The two collectors of the NPN BJT 14, 16 are connected together.

The emitter of the first NPN BJT 14 is connected to the base of the second NPN BJT 16. The first NPN BJT 14 and the second NPN BJT 16 form a NPN Darlington circuit. The base of the first NPN BJT 14 is a control end of the NPN Darlington circuit, the collector of the first NPN BJT 14 is an input end of the NPN Darlington circuit, and the emitter of the second NPN BJT 16 is an output end of the NPN Darlington circuit. The drain of the NMOS transistor 12 is connected to the input end of the NPN Darlington circuit, the gate of the NMOS transistor 12 is connected to the output end of the NPN Darlington circuit, and the source of the NMOS transistor is connected to the control end of the NPN Darlington circuit. The input end of the NPN Darlington circuit is connected to an input pad 22 of an internal circuit, and the output end is connected to ground. The first resistor 18 is connected between the base of the first NPN BJT 14 and ground. The second resistor 20 is connected between the base of the second NPN BJT 16 and ground. When the input pad 22 of the internal circuit is influenced by an electrostatic discharge, the NMOS transistor 12 is triggered to turn on immediately so that the electrostatic current flows through the first resistor 18 forming a voltage drop. The voltage drop drives the first

NPN BJT 14 to turn on so that the electrostatic current flows through the second resistor 20 forming another voltage drop. This voltage drop drives the second NPN BJT 16 to turn on to drive most electrostatic current through this loop to ground achieving the ESD protection. In this example, the emitter of the second NPN BJT 16 is designed with twice the width of the first NPN BJT 14 for achieving better ESD protection. The resistance values of the first resistor 18 and the second resistor 20 are chosen as 500 ohms for forming the voltage drops to turn on the NPN BJTs 14, 16. The width of the emitter of the first NPN BJT 14 and the second NPN BJT 16 and the resistances of the first resistor 18 and the second resistor 20 can be chosen according to practicability according to the present invention.

[0020] Please refer to Fig.4A and Fig.4B. Fig.4A and Fig.4B are cross-sectional views of a BiCMOS structure of an ESD protection circuit according to the present invention. As shown in Fig.4A, in a BiCMOS process, a P-epi layer or an N-epi layer 32 is first formed on a P-substrate 30, then an N+ buried layer 34 is embedded in the epitaxial layer 32. A P well 38 is formed on the N+ buried layer 34, and a NW+ sink 36 is injected into a perimeter of the P well 38

on the N+ buried layer 34 to isolate the P well 38 and the P-substrate 30. Lastly, an N+ node 40 is embedded in the P well 38. In said structure according to the present invention, an NPN BJT uses the N+ node 40 as an emitter, the P well 38 as a base, and the N+ buried layer 34 as a collector, as shown in Fig.4A. An NMOS transistor uses two N+ nodes 40 as a drain and a source, and an insulation layer 42 formed on the channel between the two N+ nodes 40 as a gate, as shown in Fig.4B. The NMOS transistor in the P well 38 is isolated by the NW+ sink 36 and the N+ buried layer 34, represented by a circle in the NMOS transistor 12 shown in Fig.3. Because of said specific isolated structure, the NPN Darlington circuit is capable of using the NMOS transistor as a trigger to achieve better ESD protection.

[0021] Please refer to Fig.5A and Fig.5B. Fig.5A and Fig.5B are cross-sectional views of a CMOS structure of an ESD protection circuit according to the present invention. Similarly, in a CMOS process a deep N well 52 is also utilized to isolate a P well 54 and a P-substrate 50. As shown in Fig.5A, the deep N well 52 is first embedded in the P-substrate 50, then the P well 54 is embedded in the deep N well 52. Lastly, an N+ node 56 is embedded in the P

well 54. An NPN BJT uses the N+ node 56 as an emitter, the P well as a base, and the deep N well as a collector, as shown in Fig.5A. An NMOS transistor uses two N+ nodes 56 as a drain and a source, and an insulation layer 58 formed on the channel between the two N+ nodes 56 as a gate, as shown in Fig.5B. The deep N well 52 isolates the NMOS transistor in the P well 54, represented by a circle in the NMOS transistor 12 shown in Fig.3.

[0022] Please refer to Fig.6. Fig.6 is a schematic view of an ESD protection circuit connected a source pad according to the present invention. For clear illustration, like elements in Fig.3 and Fig.6 have the same function and number. In Fig.3, the input end of the NPN Darlington circuit is connected to the input pad 22 of the internal circuit. When the input pad 22 of the internal circuit is influenced by electrostatic discharge, the ESD protection circuit 10 turns on to ground the electrostatic current. Similarly, the input end of the NPN Darlington circuit of the ESD protection circuit 10 is also capable of being connected to a source pad 24. When the source pad 24 is influenced by an electrostatic discharge, the ESD protection circuit 10 turns on to ground the electrostatic current. In general, a human-body model (HBM) and a machine model (MM) are used to

simulate the electrostatic discharge. The effect of ESD protection is estimated by measuring values of the HBM or MM, and a large value of the HBM and MM indicates better ESD protection. When an ESD protection circuit is connected to an input pad of an internal circuit, the HBM value of the prior art is 2.5KV and the MM value is 200V, however, the HBM value of the present invention is 5.5 KV and the MM value is 500V. When an ESD protection circuit is connected to a source pad of an internal circuit, the HBM value of the prior art is 5KV and the MM value is 200V, however, the HBM value of the present invention is 5 KV and the MM value is 400V. According to said data, the ESD protection circuit 10 will protect a circuit from electrostatic discharge effectively.

[0023] Please refer to Fig.7. Fig.7 is a schematic view of a complementary ESD protection circuit according to the present invention. In Fig.3, if the source receives an electrostatic discharge pulse, the electrostatic current has to flow to the input pad 22 of the internal circuit through ground and the effect of the ESD protection may not satisfy higher requests. As shown in Fig.7, a circuit 26 completely complementary to the ESD protection circuit 10 in Fig.3 composed of PNP BJTs and a PMOS transistor is added be-

tween the source and the input pad 22 of the internal circuit. If the source receives an electrostatic discharge, the electrostatic current flows to the input pad 22 of the internal circuit through the circuit 26 directly to enhance the effect of ESD protection.

[0024] In contrast to the prior art, the ESD protection circuit 10 according to the present invention uses an N well 36 and an N+ buried layer 34 to isolate the NMOS transistor in the P well 38 in a BiCMOS application, and uses a deep N well 52 to isolate the NMOS transistor in the P well 54 in a CMOS application. Because of said isolation technique, the NPN Darlington circuit composed of the NPN BJTs 14, 16 is capable of using the NMOS transistor 12 as a trigger to drive the NPN Darlington circuit to ground the electrostatic current so that ESD protection is better. Experimentation has confirmed that the ESD protection circuit according to present invention is more effective than the prior art no matter the protection circuit connects to the source pad or the input pad of the internal circuit.

[0025] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited

only by the metes and bounds of the appended claims.